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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H01L 27/115, 29/51, G11C 11/22, C04B 35/46 — A1

(11) International Publication Number: WO 00/49659

(43) International Publication Date: 24 August 2000 (24.08.00)

(21) International Application Number: PCT/IB00/00043

(22) International Filing Date: 17 January 2000 (17.01.00)

(30) Priority Data:
PCT/IB99/00283 17 February 1999 (17.02.99) IB

(71) Applicant *(for all designated States except US)*: INTERNATIONAL BUSINESS MACHINES CORPORATION [US/US]; New Orchard Road, Armonk, NY 10504 (US).

(72) Inventors; and

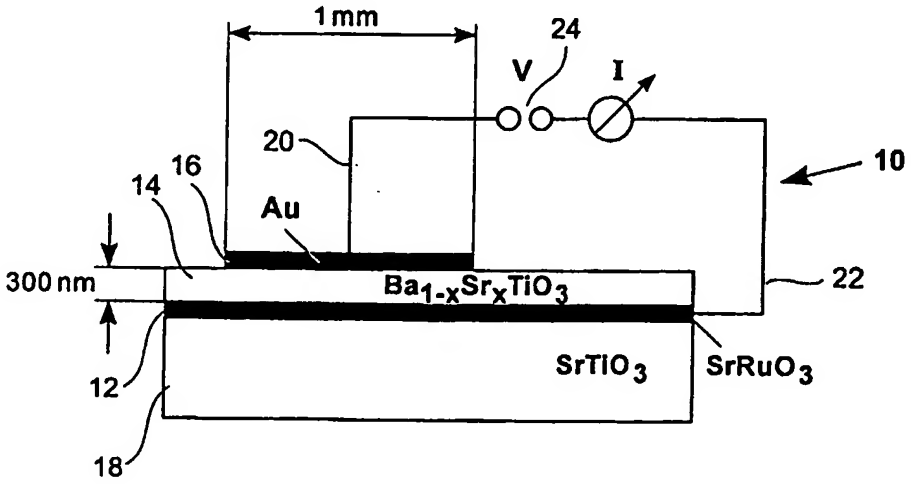
(75) Inventors/Applicants *(for US only)*: BECK, Armin [DE/CH]; Alte Steinacherstrasse 25, CH–8804 Au (CH). BEDNORZ, Johannes, G. [DE/CH]; Herschaerenstrasse 89, CH–8633 Wolfhausen (CH). GERBER, Christoph [CH/CH]; Im Gruet 2, CH–8805 Richterswil (CH). ROSSEL, Christophe, P. [CH/CH]; Im Langacher 25, CH–8805 Richterswil (CH).

(74) Agent: HEUSCH, Christian; International Business Machines Corporation, Säumerstrasse 4, CH–8803 Rüschlikon (CH).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: MICROELECTRONIC DEVICE FOR STORING INFORMATION AND METHOD THEREOF



(57) Abstract

The basic discovery underlying the present invention concerns a plurality of oxide substances, i.e., materials for use in microelectronic and in electronic circuits and particularly semiconductor chips which combine both a switching phenomenon in resistance and a built–in memory. One preferred member of that plurality is $Ba_xSr_{1-x}TiO_3$ with $0 \leq x \leq 0.7$ and having a dopant of Chromium between 0 % and 5 %, preferably between 0 % and 1 %, even more preferably about 0.2 %. When said substance is used for example as a dielectric layer in a capacitor–like structure it stays switched in either a high or a low conductivity state depending on the voltage pulse being applied to it. Thus it is possible to store digital information by different values of resistance, i.e., by associating a high resistance state with a logic "0" and a low resistance state with a logic "1". Such stored information can be read out by measuring the leakage current. Even multi–level switching is realizable.

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MICROELECTRONIC DEVICE FOR STORING INFORMATION AND METHOD THEREOF

1. BACKGROUND OF THE INVENTION

1.1 FIELD OF THE INVENTION

The present invention relates to electronic and microelectronic devices. In particular, the present invention relates to a plurality of materials showing a switching phenomenon and a built-in memory by the aid of which a new principle of storing and reading information in memory cells of semiconductor chips and a plurality of fundamental improvements on electronic or microelectronic devices can be achieved.

1.2 DESCRIPTION AND DISADVANTAGES OF PRIOR ART

Although the present invention is applicable in a broad variety of microelectronic or electronic applications it will be described with the focus put on an application to memory cells as RAM (Random Access Memory), for example.

The need to remain cost and performance competitive in the production of semiconductor devices has caused continually increasing device density in integrated circuits. To facilitate the increase in device density, new technologies are constantly needed to allow the feature size of these semiconductor devices to be reduced.

Conventional DRAM cells, whereby DRAM stand for Dynamic Random Access Memory, consist of a transistor and a capacitor mostly made from Silicon dioxide (SiO_2). They need the transistor to control the inflow and outflow of charge stored in the capacitor as the physical quantity exploitable for storing information. Said transistor also decouples the capacitors from each other. Such DRAM cells have the disadvantage, that information stored therein is volatile and as such can principally be lost on each power supply failure. Further, the time needed to refresh the information

contained in DRAM cells delimits the read and write performance of such cells. Finally, the structure of such a DRAM cell is quite complex due to the required transistor.

Thus, a change in computer RAM technology beyond conventional DRAM technology would be desirable.

The use of ferroelectric non-volatile RAM (NVRAM) cells would already be a great step forward as information would not be lost on any power failure although the structure of the memory cell would remain complex, too. In such ferroelectric RAMs the polarization of the bit storing layer is exploited instead of a capacitor's capacity in DRAM cells for defining two different states which can be associated with two different logical values. A long term repetitive switching between two different states of remanent polarization, however, fatigues the ferroelectric properties of the material, as e.g. lead zirconium titanate (PZT).

In 'Physics Today' July 1998, page 24 a further high permittivity material and a respective semiconductor fabricating technology is proposed which allows the computer industry to use the equipment of its conventional DRAM manufacturing plants without having to perform basic retooling. It is the so-called high permittivity DRAM technology.

Herein, the charge of a capacitor can be used to store information as it is done in conventional DRAM technology as the polarization of a high permittivity layer depends linearly on the applied voltage, as required for charging the DRAM capacitors. A high permittivity material as e.g. barium strontium titanate (BST) having a permittivity ε_r about 500 instead of ε_r about 4 for silicon dioxide would allow to reduce the space needed for the capacitor as its capacitance is proportional to its area and the magnitude of its permittivity value. This in turn would allow higher integration levels compared to conventional silicon oxide materials used in DRAM cells as the capacitor's area consumption is large as compared to that of the coupled transistor.

But, nevertheless, as a disadvantage remains that the leakage current is still significant. Thus, refreshing is a must.

Investigations in the sixties at oxide diodes and thin oxide films revealed several phenomena. For example, J. F. Gibbons and W. E. Beadle reports in their article "Switching properties of thin NiO films", Solid-State Electronics, Pergamon Press 1964, Vol. 7, pp. 785-797, about a two-terminal solid-state switch made from a thin film of nickel oxide. After about 100 - 1000 switching cycles, the device could not be switched out of an ON condition with normal switching signal amplitudes. Other tests on oxide diodes were performed whereby switching was induced by applying high voltages. These diodes broke down after a few cycles and became unusable. T.W. Hickmott reports in Applied Physics Letters, Vol. 6, No. 6, on page 106 and in the Journal of Vacuum Science and Technology, Vol. 6, No. 5 on page 828 about bistable switching in Niobium oxide diodes. He noticed that the metal electrode plays an important role. To sum up, the tested devices and materials showed that they were either difficult to control or unreliable.

In US Patent No. 4,931,763 a memory switch is described that bases on metal oxide thin films. The memory switch is irreversible and therefore only switches once. It can be used as connection element in circuits and arrays but not for storing of changing information.

Finally, with increasing integration near and beyond the 1 Gbit chip due to smaller capacitor size the area consumption of the transistor of a memory cell is not negligible anymore. Thus, a great step forward to Ultra Large Scale Integration (ULSI) would be to simplify the structure of a memory cell as much as possible.

1.3 OBJECTS OF THE INVENTION

Therefore, an object of the present invention is to provide a robust simply structured, reliable and non-volatile memory cell.

It is another object of the present invention to provide a new simpler method for stable storage of information into such a memory cell and a reproducible erasing and reading from it.

It is another object of the present invention to provide a simply structured and non-volatile memory cell which is able to store more than only two distinct values, i.e., which is usable for multilevel storage.

2. SUMMARY AND ADVANTAGES OF THE INVENTION

These objects of the invention are achieved by the features stated in enclosed independent claims. Further advantageous arrangements and embodiments of the invention are set forth in the respective subclaims.

The basic discovery underlying the present invention concerns a plurality of doped oxide substances including perovskites and related compounds, i.e. materials, for use in microelectronic devices and in electronic circuits and particularly for use in semiconductor chips which combine both, a switching phenomenon in resistance and a built-in memory.

A microelectronic device can be designed such that it comprises a region between electrodes with switchable ohmic resistance wherein the region is made of a substance comprising components A_x, B_y, and oxygen O_z. The ohmic resistance in the region is reversibly switchable between different states by applying different voltage pulses. The different voltage pulses lead to the respective different states. An appropriate amount of dopant(s) in the substance improves the switching, whereby the microelectronic device becomes controllable and reliable.

In general and coinciding with the wording of the claims substances are meant comprising components A_x, B_y, and oxygen O_z, in which substance said component A is a member of Alkaline metals (group IA in the periodic system of elements), or Alkaline Earth metals (group IIA), or Rare Earth elements, or Scandium, or Yttrium, said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA and the substance has a crystalline structure.

Generally, an elementary cell of the corresponding lattice structure comprises a cell center molecule which is surrounded by a plurality of oxygen-molecules each having in turn a center molecule. Both types of said center locations can principally be taken by either of the component A, or B, respectively. In other words, there are a plurality of

substances, i.e., where chemically appropriate, in which A and B can change their locations. In view of the large plurality of the different usable substances this understanding of the basic formula given above should be stressed in order to assure the intended scope and to conserve clarity and conciseness of the appended claims, concurrently.

Said substances comprise some specific range of amount of a dopant of one of or a combination of Chromium, Vanadium, or Manganese, or further transition metals.

In particular, any substance comprising components A_x, B_y, and oxygen O_z, in which substance said component A is a member of Alkaline metals (group IA), or Alkaline Earth metals (group IIA), or Rare Earth elements, or Scandium, or Yttrium, and said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA are substances which are able to solve the problem underlying to the present invention, when doped with a dopant of one of or a combination of transition metals, in particular but not exclusively with Chromium, Vanadium, or Manganese, the total dopant amount being larger than 0% and smaller than 5%, and preferably about 0.2% when $(BaSr)TiO_3$ is doped with Chromium only. Other preferred amounts of dopants are specific for each dopant element used and substance to be doped.

Having found the appropriate amount of dopant(s), a stable switching behavior required to operate a microelectronic device, such as a memory cell, can be provided. Fast write, read and erase processes, similar to time scales that are reached with conventional dynamic memories, are achievable.

Some additional specific requirements should be met by the combination of indices x, y, z in order to find the substances adapted to the present concept. Each of the following items define a subclass of substances which show the desired switching effect:

The combinations of indices x, y and z being defined by

$x = n + 2$, $y = n + 1$, $z = 3n + 4$, with $n = 0, 1, 2, 3$ reveal the so-called Ruddlesden

the so-called perovskites, like $SrTiO_3$, $BaTiO_3$, $KNbO_3$, $LiNbO_3$, and others,

for n = 2 Sr_2FeMoO_6 and similar substances are provided having a (226) index sequence.

The combinations of indices x, y and z being defined by
$x = n + 1$, $y = n$, $z = 4n + 1$, with n = 1, or 2 reveal a separate class of substances.

For n = 1 substances having an index sequence (215) like Al_2TiO_5, Y_2MoO_5 and others are provided, and

$SrBi_2Ta2O_9$ and similars are provided for n = 2.

Each of the classes mentioned above can be modified by varying the composition of the substance in order to achieve that at least one of said components A_x or B_y, respectively, is comprised of a combination of elements out of one group or out of several of the corresponding groups of A, and B, respectively.

A further modification is provided by providing a superlattice made by a combination of structural unit cells and/or sub-unit cells as it is published in 'E. Kaldis et al. (eds.), High-Tc Superconductivity 1996: Ten Years After Discovery, pp. 95-108', having each a different n, and in which structural unit cells and/or sub-unit cells are each a member of a corresponding homologous series obtained by oxygen intercalation. A further modification is provided by providing a superlattice made by a combination of structural unit cells and/or sub-unit cells of the Ruddlesden-Popper type structures having each a different n, and in which said structural unit cells and/or sub-unit cells are each a member of a corresponding homologous series. In said lattice modifications lattice structures are formed in which single or multiple transition metal oxygen octahedra layers are separated by one or more block layers consisting of component A and oxygen.

One preferred member of that plurality of substances is $Ba_xSr_{1-x}TiO_3$ with $0 <= x <= 0.7$ and having a dopant amount of Chromium between 0% and 5%, preferably between 0 and 1%, even more preferably about 0.2%.

Others members of that plurality are materials according to $Ba_xSr_{1-x}TiO_3$ with $0 <= x <= 0.7$ and having a dopant of Vanadium between 0% and 5%.

Manganese is a preferred dopant, too, particularly in composition with Chromium or Vanadium.

Further members of that plurality are perovskite related compounds with other transition metal cations such as Nb. Further dopants can be transition metal elements and combinations thereof, i.e., elements having their valence electron(s) on the d-orbital, i.e., 3d, 4d, or 5d -orbital.

When such a material is used for example as a dielectric layer in a capacitor-like structure to form the microelectronic device, it stays switched in either a high or a low conductivity state depending on a voltage pulse being applied to it until it is switched into the other state by applying a new voltage pulse. Thus, said capacitor-like structure having such a complex dielectric material has a resistance which can be varied by applying short voltage or, alternatively, short current pulses to the embedding electrodes.

As the most decisive electrical property of such a microelectronic device is the change in resistance depending on a defined, applied voltage pulse between the two terminals of the microelectronic device, whereby said capacitor-like structure can be regarded as a 'switchable resistor'. Said switching behavior is known to be effectuated by a voltage or current driven hysteresis behavior.

Due to said property it is possible to store digital information by different values of resistance, i.e., by associating a high resistance state with a logic '0' and a low resistance state with a logic '1'. The actual state and thus the stored information can be read out by a current readout or measuring the leakage current as it is relatively large

with low resistance of the dielectric layer and vice versa. Thus, the leakage current which impedes the performance of prior art DRAM technology can be usefully taken for reading the stored value. According to the invention neither the static charge of a capacitor nor the polarization of any ferroelectric material is needed to be used for storing information but, instead, its resistance.

Thus, a simple way to store information can be followed by realizing the above mentioned concept.

The material usable in connection with the present invention when used for e.g. RAM cells has the advantage, in relation to prior art memory cells, that new cells can be constructed just comprising a single capacitor-like structure device with only one pair of electrode terminals for operating it, i.e. to read from, to write into or to erase without a transistor arrangement being necessarily coupled with a capacitor used in prior art to perform the operating functions of a prior art DRAM cell. One terminal of such a cell is connected to ground and the other is used for writing, erasing or just reading.

Thus, RAM cells can be constructed to use considerably less space on a chip and considerable less manufacturing steps.

Further, the usable material has a remarkable high retention time of at least several months with no power connected and can thus be used as a non-volatile memory. Thus a double advantage can be achieved: first, the full time is available for the read and write processes because the refresh cycles and therefore the refresh circuitry are not required anymore and, secondly, a data storage security is increased as a loss of power supply does not imply a loss of stored data.

Basically, the memory cell can be operated in either a voltage controlled or in a current controlled regime, i.e. information can be stored by applying voltage pulses or by applying current pulses. In both cases the information can be read by sensing voltage or current. For purposes of improved clarity of this disclosure, however, only the voltage regime is described in the detailed description down below.

Finally, for example in the voltage controlled mode the current flowing when reading a '1' compared to that one when reading a '0' value is about 20 times larger due to the difference in resistance. This feature can advantageously be used for storing more than only one bit in the same cell. Thus, a plurality of two, three, or more bits can be stored or removed by applying different voltage pulses, single pulses or sequences thereof having different shape, level, or duration or being different in number to write and erase. A sufficiently large distance between the different levels can hereby be maintained.

3. BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and is not limited by the shape of the figures of the accompanying drawings in which:

Fig. 1 is a schematic drawing of a perovskite oxide capacitor-like structure of a microelectronic device usable as memory cell,

Fig. 2 shows current-voltage characteristics of a 300 nm thick Cr doped oxide capacitor-like structure,

Fig. 3a to 3c show the principles of operation of the capacitor-like structure analyzed in Fig. 2 as a memory device,

Fig. 4a to 4c show the operation of a further microelectronic device as a multilevel memory device,

Fig. 5a to 5h show results of measurements over an extended time period, and

Fig. 6 shows a schematic circuit diagram representing the arrangement of a 4-bit-memory circuit.

4. DESCRIPTION OF THE PREFERRED EMBODIMENT

With general reference to the figures and with special reference to Fig. 1 the essential structure of a microelectronic device 10 having a capacitor-like structure is described in more detail. Such a microelectronic device 10 is useable as a memory cell.

The microelectronic device 10 comprising an oxide base electrode 12 made from $SrRuO_3$ and a region 14 with an oxide insulator layer made from $(BaSr)TiO_3$ slightly doped with Chromium (Cr) for the insulating material and a metallic (Au) top electrode 16 on a $SrTiO_3$ substrate 18 was fabricated with pulsed laser deposition. The microelectronic device 10 has a thin film capacitor-like structure.

One terminal 20 is connected to said top electrode 16, the other terminal 22 is connected to said base electrode 12.

In an experimental arrangement setup for testing the basic switching behavior and further physical properties of the microelectronic device 10 the insulator layer thickness was 300 nanometers.

The insulator layer of the region 14 was doped with Chromium (Cr) at an amount of 0.2%.

The leakage current was measured as it is depicted in the drawing as a function of the bias voltage generated by a DC voltage source 24 between said terminals 20, 22.

With respect to Fig. 2a to 2c the leakage current voltage characteristic is illustrated in Fig. 2a linearly, in Fig. 2b with a logarithmic leakage current scale of its absolute amount and in Fig. 2c with both logarithmic scales.

For small applied bias voltages like several 10 mV a linear current voltage characteristic (IVC) can be observed. A quadratic dependence of the current from the applied voltage can be seen for moderate applied voltages as several 100 mV.

This IVC shape and behavior can be described as space charge limited current. Larger applied voltages result in an exponential like rise of the leakage current with increasing applied voltages.

The capacitor-like structure of the microelectronic device 10 shows a reproducible switching behavior causing a hysteresis loop in the current voltage characteristic, described next below:

A large negative bias voltage -negative with respect to the $SrRuO_3$ electrode- leads to a sudden increase of the leakage current, depicted at about - 0.8 Volt. Sweeping back to large positive bias voltage the leakage current drops back to a low value again depicted at + 0.7 Volt. Said sudden increase and said sudden drop back of leakage current are essential features for switching and deciding between different states.

According to the invention it is possible to operate the microelectronic device 10 as a very simple device or memory device, i.e. memory cell in a RAM due to and with the described underlying switching behavior. This will be illustrated in conjunction with Figs. 3a to 3c and 4a to 4c.

Basically, by applying a write voltage pulse to the microelectronic device 10 the system is switched into a low resistance state which can be regarded as storing information. An erase voltage pulse recovers the resistance state of the microelectronic device 10 and the information is removed, i.e. erased.

As can be seen in Fig. 3a a series of 300 ms long different voltage pulses depicted as sharp peaks were applied to the electrodes (12,16) of the microelectronic device 10.

A write pulse, also called second voltage pulse 6.1, that here is a negative pulse is used to write information which after a certain delay is removed by an erase pulse, also called first voltage pulse 5.1, that here is a positive pulse. In general, each first voltage pulse 5.1 leads to a first state 1, a high ohmic state, and on the other hand each second

voltage pulse 6.1 leads to a second state 2, a low ohmic state, as can be seen from Fig. 3a in conjunction with Fig. 3c. Between the repeating voltage pulses 5.1, 6.1 a small negative read voltage 9 is switched on and off periodically to read the information and to simulate a realistic readout process. 120 reading cycles each having a duration of 1 sec are performed after each write or erase pulse. This readout procedure is schematically depicted in a better time resolution by the zoomed portion in Fig. 3a.

The readout from the microelectronic device 10 is performed by measuring the leakage current flowing at a small applied voltage of - 0.2 V as it is depicted in Fig. 3b which shows current spikes occurring during write and erase followed by the readout period with currents one order of magnitude lower. Fig. 3c is a leakage current scale enlargement of Fig. 3b and clearly shows the above-mentioned first state 1 and second state 2.

Two different resistance states can be clearly separated: The first state 1 around 30 nano Amperes yielding a resistance of R = 6.6 Mega Ohm and the second state 2 having a leakage current of 650 nano Amperes yielding a resistance of R = 300 kilo Ohm. The first state 1 will now be associated with a logic state '0' and the second state 2 with a logic state '1'.

The '1' resistance value is 20 times smaller than the '0' value. A clear separation of the two logic states '1' and '0' is thus achieved.

Additionally, this remarkable dependence of the resistance on the applied voltage pulse 5.1, 6.1 together with the hysteretic behavior also allows to write different values to the microelectronic device 10 and to read them out with a single pre-specified read-out voltage. This so-called multi-level switching phenomenon is discussed later in more detail.

During the experimental measuring runs in this example information was written and erased during 300 ms - the duration of the sharp peaks - and stored for 240 s. The time to write and erase information was a specifically selected experimental parameter but is

not limited by the memory device itself. Therefore, the ultimate speed for the write/erase process is much higher, as shown with reference to Fig. 5.

The time over which information can be stored is much longer than those 240 s measured experimentally, as further measurements confirmed that are shown in Fig. 5.

If one analyzes the switching behavior of such capacitor-like structures with varying Cr doping it can be observed that the switching behavior is more pronounced for slightly Cr doped structures, i.e. the best results are obtained with Cr-doping around 0.2%. For these capacitor-like structures the difference between '0' and '1' was the best with adequate reproducibility.

Summarizing the main aspects of the presented structure having a DC-resistance changing sensitively with the applied voltage pulses and consisting of oxides doped can be operated as a memory device or cell with the following intriguing properties:

First they have a very simple structure because the whole memory cell is a capacitor-like structure. Thus they can be operated with only two terminals with a single terminal for read, write and erase. Thus, they are best adapted for ULSI technology.

Further, the difference in resistance between the '0' value and '1' value is at least one order of magnitude as can be seen from Fig. 3c. As can be seen further from the IVC depicted in Fig. 2a, a large resistance range can thus be exploited to store a plurality of different logical values, i.e., the so-called multilevel switching can be achieved. For this, a plurality of write pulses different in size, etc., as mentioned earlier can be applied to write specific logical values into the memory cell, in order to realize not a binary system but, e.g., a digital decimal system based on 10 different logical values being able to be written into and to be read from said memory cell in subsequent write/ read/erase cycles.

Finally, the information is stored over long times which is a remarkable advantage compared to conventional DRAM cells.

Fig. 4a to 4c show the operation of a further microelectronic device, a second memory device, that can be used as a multilevel memory device. Since the Fig. 4a to 4c are related to each other, they will be regarded in context to understand the operation of the second memory device. This second memory device for the sake of simplicity is not depicted but is structured as shown in Fig. 1. The second memory device comprising an oxide base electrode 12 made from $SrRuO_3$ and a region 14 made from $SrZrO_3$ slightly doped with 0.2% Chromium (Cr) for the insulating material and a metallic (Pt/Ti) top electrode 16 on a $SrTiO_3$ substrate 18 was fabricated with pulsed laser deposition again.

As can be seen in Fig. 4a a series of different voltage pulses depicted as sharp peaks were applied to the second memory device. In particular, erase voltage pulses 5, low write pulses 6, medium write pulses 7, and high write pulses 8 were applied in a defined repeating sequence in order to simulate realistic erase and write processes. Each peak of the erase voltage pulses 5 indicates 30 pulses with a duration of 1 ms. A small read voltage 9 were applied appropriately in intervals of 10 s in order to read information. This read voltage 9 is smaller in magnitude than the different voltage pulses 5, 6, 7, 8 applied for switching to different states 1, 2, 3, 4.

Fig. 4b shows the current generated by the different voltage pulses 5, 6, 7, 8 and Fig. 4c the current readout enlargement of Fig. 4b. Different states 1, 2, 3, 4 corresponding to different ohmic resistances can be clearly derived from Fig. 4c. The ohmic resistance of the region 14 of the second memory device can be regarded as 'high' after one erase pulse 5 has been applied, that means that the second memory device then stores a high ohmic state, also referred to as first state 1. Conversely, each low write pulse 6 leads to a second state 2, each medium write pulse 7 leads to a third state 3, and each high write pulse 8 leads to a fourth state 4 whereby this fourth state 4 is the lowest ohmic state. The second state 2 and the third state 3 are in-between the high ohmic and the lowest ohmic state. As can be seen in Fig. 4a erase pulses 5 were applied between the write

pulses 6, 7, 8 to switch respectively from the second state 2, the third state 3, or the fourth state 4 to the first state 1.

With each of the different states 1, 2, 3, 4 a corresponding logical value can be associated, e.g., the first state 1 corresponds to logical '00', the second state 2 corresponds to logical '01', the third state 3 corresponds to logical '10' and the fourth state 4 corresponds to logical '11', representing a 2 bit memory cell. In general, more states are possible than the depicted four different states 1, 2, 3, 4.

The erase voltage pulses 5 are here negative voltage pulses whereas the write pulses 6, 7, 8 are positive pulses. Basically, before a memory device is used the first time, an initializing voltage should be applied to polarize this device. Depending on this polarization the erase voltage pulses might either be positive and the write pulses negative or the erase voltage pulses are negative and the write pulses are positive.

It shows advantageously, if each of the erase pulses 5 has an equal or smaller magnitude of the amplitude of the write pulses 6, 7, 8.

Contrary to the example, the erase pulses 5 can have different amplitudes for switching directly from the fourth state 4 to the different states 3, 2, 1 having higher ohmic resistance. That means, in particular, for switching from a low ohmic state, that here is the fourth state 4, to a higher ohmic state, e.g. the third state 3, the second state 2, or even the first state 1, the erase pulses 5 have an adapted step-like increased amplitude. Also possible in such a way is a switching from the fourth state 4 directly to the second state 2.

The switching behavior of the multilevel memory device was investigated and tested at 77 K, whilst the same switching behavior can be realized at room temperature.

Fig. 5a to 5h show results of measurements over an extended time period on another microelectronic device, a third memory device. This third memory device has the same structure as the second memory device as described above with the exception that the top electrode 12 comprises Au.

In general, within the uppermost row of figures the applied voltages are depicted whilst in the bottom row of figures the resulting current readouts are shown. Fig. 5a indicates two erase pulses 5 and three write pulses 6, each of a duration of 1 µs and applied in intervals of 1 min. The current readout with the corresponding states 1, 2 are depicted in Fig. 5b. A third positive write pulses 6 on the 28.4.99 leaded to a switch from the first state 1 to the second state 2, as can be seen from the figures. After that, the third memory device was stored without any power connection and not used for a longer period of time. Fig. 5c and 5d indicate unperiodical measurements within a time period of two month, whereby the measuring dates are listed in Fig. 5d. More particular, Fig. 5c indicates the read voltage pulses 9 whereas Fig. 5d depicts the current readout result. The result shows that the second state 2 was stored over a longer period of time and thus the third memory device can be regarded as non-volatile for this time period. Fig. 5e shows further write and erase pulses, respectively, and Fig. 5f the resulting states. Finally, Fig. 5g and 5h indicates further unperiodical measurements within a time period of three month, whereby the measuring dates are named in Fig. 5h. On one hand Fig. 5g depicts the read voltage pulses 9 again whereas on the other hand Fig. 5h shows the resulting current readout. The measurements show again that the last information stored in the third memory device was stored over a longer period of time without any decay.

With reference to Fig. 6 a schematic circuit diagram representing the arrangement of a 4-bit-memory circuit is shown.

Four microelectronic devices 10, also referred to as memory cells 10, are arranged linearly in order to represent the 4-bit-memory circuit addressed via an address line 28 by a decoder 30 the outputs of which are connected to a respective top electrode 16, as shown in Fig. 1. The base electrodes 22 thereof are each connected to ground. A write, erase, or read voltage pulse can be applied to a selected memory cell 10 through a bias line 32. The different memory cells output current is evaluated through the output line 34.

In a similar way a matrix like arrangement can be achieved by connecting the base electrodes 22 of a row of the memory cells 10 with a further decoder.

It is obvious that the arrangement of the particular components 12, 14, 16, 18 of the capacitor-like structure on a chip, as shown in Fig. 1, will be adapted to the requirements imposed by the specific integration level which is intended to be achieved with the chip. A broad spectrum of different architectures can thus be realized.

Beside the capability of the memory cells 10 described above to store information it is possible to use a system comprising an doped capacitor-like structure as an active switching element in electric or electronic circuits.

In this area of interest a switching operation is not restricted to a specific resistance value. Devices having a resistance of some Mega Ohms can be operated at a voltage between 1 Volt and 5 Volt for writing and erasing and at a voltage between 0.05 Volt and 0.5 Volt for reading. Devices having a smaller resistance can also be operated, however at different voltages.

Further, the present concept is suitable for an application of the substance for constructing EEPROMs (Electrically Easable Programmable Read Only Memories), logic gates as e.g. AND gates, OR-gates, tunable capacitors and further complex logic circuits.

Particularly, when silicon (Si) or other semiconductor substrates are taken as substrate material instead of strontium titanate the current prior art semiconductor materials can be grown on the substrate thus providing the ability to join conventional semiconductor technology with the memory cells or switching elements, respectively, of the present concepts.

In the foregoing specification the invention has been described with reference to a specific exemplary embodiment thereof. It will, however, be evident that various modifications particularly relative to the application of a large variety of different

substances as they are mentioned in the appended claims may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims.

The specification and drawings are accordingly to be regarded as illustrative rather than in a restrictive sense.

In particular the thickness of the region 14 as well as the lateral dimensions of a memory cell and the applied bias voltages or bias currents, respectively, can be varied as it is required by any specific purpose imposed by any of a plurality of varying chip designs.

Also the material selection for the bottom electrode can be varied as well. A simple metal like platinum (Pt) is suited as well.

Also for the top electrode the material can be varied as well. Au, Pt are suited materials, but principally, all metals and conducting oxides are suited materials for both, top and bottom electrodes.

CLAIMS

1. A microelectronic device having a region (14) between electrodes (12, 16) with switchable ohmic resistance, wherein the ohmic resistance in said region (14) is reversibly switchable between different states (1, 2, 3, 4) by applying different voltage pulses (5, 5.1, 6, 6.1, 7, 8) leading to said different states (1, 2, 3, 4) and wherein said region (14) is made of a substance comprising components A_x, B_y, and oxygen O_z, in which substance
said component A is a member of Alkaline metals (group IA), or Alkaline Earth metals (group IIA), or Rare Earth elements, or Scandium, or Yttrium,
said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA,
said substance comprises a dopant of one of or a combination of different transition metals, the total dopant amount being larger than 0% and smaller than 5%.

2. The microelectronic device according to claim 1, wherein the ohmic resistance in the region (14) is switchable between at least a first state (1) of the different states and a second state (2) of the different states by applying to the electrodes (12, 16) a first voltage pulse (5.1) of the different voltage pulses for switching from said second state (2) to said first state (1) or a second voltage pulse (6.1) of the different voltage pulses for switching from said first state (1) to said second state (2).

3. The microelectronic device according to claim 2, wherein the ohmic resistance in the first state (1) is higher than in the second state (2) and wherein the first voltage pulse (5.1) of the different voltage pulses for switching to said first state (1) has an opposite sign to the second pulse (6.1) of the different voltage pulses for switching to said second state (2).

4. The microelectronic device according to claim 1, wherein each of the different states (1, 2, 3, 4) is obtainable by an erase pulse (5) for switching the ohmic resistance in the region (14) to a high ohmic state (1) of the different states and/or at least one write pulse (6, 7, 8) for switching from said high ohmic state (1) to a lower ohmic state (2, 3, 4) of the different states .

5. The microelectronic device according to claim 4, wherein the erase pulse (5) has different amplitudes for switching to one of the lower ohmic states (2, 3, 4).

6. The microelectronic device according to one of claims 1 to 4, wherein the different states (1, 2, 3, 4) are readable by a read voltage (9) smaller in magnitude than the different voltage pulses (5, 5.1, 6, 6.1, 7, 8) applied for switching to the different states (1, 2, 3, 4).

7. The microelectronic device according to claim 1 being usable as a capacitor-like structure, wherein the region (14) represents a dielectric.

8. The microelectronic device according to claim 1, whereby a specific ohmic resistance of the region (14) related to one of the different states (1, 2, 3, 4) remains after one of the different voltage pulses (5, 5.1, 6, 6.1, 7, 8) that leads to said specific ohmic resistance has been applied to the electrodes (12, 16).

9. The microelectronic device according to one of the preceding claims being able to store digital information that is representable by different values in ohmic resistance of the region (14), thereby preferably storing two or more bits as digital information.

10. The microelectronic device according to claim 1, in which the combinations of indices x, y and z of the substance are definable by

$x = n + 2, y = n + 1, z = 3n + 4$, with $n = 0, 1, 2, 3$; or

$x = n + 1, y = n + 1, z = 3n + 5$, with $n = 1, 2, 3, 4$.

11. The microelectronic device according to claim 1, in which the combinations of indices x, y and z of the substance are definable by either of:
x = 1, y =1, z = 1, and one of the indices x or y being 0; or
x = n, y = n, z = n + 1, with n = 1 or 2 and one of the indices x or y being 0; or
x = n, y = n, z = 2n + 1, with n = 2 and one of the indices x or y being 0.

12. The microelectronic device according to claim 1, in which the combinations of indices x, y and z of the substance are definable by
x = n, y = n, z = 3n, with n = 1, or 2, or 3; or
x = n + 1, y = n, z = 4n + 1, with n = 1, or 2.

13. The microelectronic device according to claim 1, comprising a dopant of Chromium or Vanadium at an amount larger than 0% and smaller than 5%, preferably about 0.2%.

14. The microelectronic device according to claim 1, wherein at least one of the components A_x or B_y of the substance comprises a combination of elements out of one group or out of several of the corresponding groups of A, and B, respectively.

15. The microelectronic device according to claim 11, wherein the substance is present in the form of a superlattice made by a combination of structural unit cells and/or sub-unit cells.

16. The microelectronic device according to claim 10 or 12, wherein the substance is present in the form of a superlattice made by a combination of structural unit cells and/or sub-unit cells having each a different n, said structural unit cells and/or sub-unit cells being each a member of a corresponding homologous series.

17. A memory cell arrangement comprising a microelectronic device according to one of the preceding claims 1 to 16.

18. A semiconductor device comprising a microelectronic device according to one of the preceding claims 1 to 16.

19. A method for writing information into a memory cell arrangement according to claim 17 comprising the step of:
applying one voltage pulse of the different voltage pulses (5, 6, 7, 8) to the electrodes (12, 16) of said memory cell arrangement for writing information into it.

20. The method according to claim 19, wherein the ohmic resistance in the region (14) is switched between at least a first state (1) of the different states and a second state (2) of the different states by applying to the electrodes (12, 16) a first voltage pulse (5.1) of the different voltage pulses for switching from said second state (2) to said first state (1) or a second voltage pulse (6.1) of the different voltage pulses for switching from said first state (1) to said second state (2).

21. The method according to claim 20, wherein the ohmic resistance in the first state (1) is higher than in the second state (2) and wherein the first voltage pulse (5.1) for switching to said first state (1) has an opposite sign to the second voltage pulse (6.1) for switching to said second state (2).

22. The method according to claim 19, wherein each of the different states (1, 2, 3, 4) are obtained by an erase pulse (5) for switching the ohmic resistance in the region (14) to a high ohmic state (1) of the different states and/or at least one write pulse (6, 7, 8) for switching from said high ohmic state (1) to a lower ohmic state (2, 3, 4) of the different states corresponding to said write pulse (6, 7, 8).

23. The method according to claim 22, wherein the erase pulse (5) has different amplitudes for switching to one of the lower ohmic states (2, 3, 4).

24. A method for reading information out of a memory cell arrangement according to claim 17 comprising the steps of:

applying a read voltage (9) to said memory cell arrangement and

associating with this information a value of current flowing through said memory cell arrangement; or

applying a current pulse to said memory cell arrangement and

associating with this information a value of voltage appearing between the electrodes (12, 16) of said memory cell arrangement.

25. Use of a substance comprising components A_x, B_y, and oxygen O_z, for making a region (14) having a switchable ohmic resistance within a capacitor-like structure, in which substance

said component A is a member of Alkaline metals (group IA), or Alkaline Earth metals (group IIA), or Rare Earth elements, or Scandium, or Yttrium,

said component B is a transition metal being member of one of the groups IB to VIII, or a member of one of the groups IIIA, IVA, VA,

said substance comprises a dopant of one of or a combination of different transition metals, the total dopant amount being larger than 0% and smaller than 5%.

26. Use of a substance according to the preceding claim, whereby the combinations of indices x, y and z are defined by

$x = n + 2$, $y = n + 1$, $z = 3n + 4$, with $n = 0, 1, 2, 3$; or

$x = n + 1$, $y = n + 1$, $z = 3n + 5$, with $n = 1, 2, 3, 4$; or

being defined by either of:

$x = 1$, $y = 1$, $z = 1$, and one of the indices x or y being 0, or

$x = n$, $y = n$, $z = n + 1$, with $n = 1$ or 2 and one of the indices x or y being 0, or

$x = n$, $y = n$, $z = 2n + 1$, with $n = 2$ and one of the indices x or y being 0; or

being defined by

$x = n$, $y = n$, $z = 3n$, with $n = 1$, or 2, or 3; or

$x = n + 1$, $y = n$, $z = 4n + 1$, with $n = 1$, or 2.

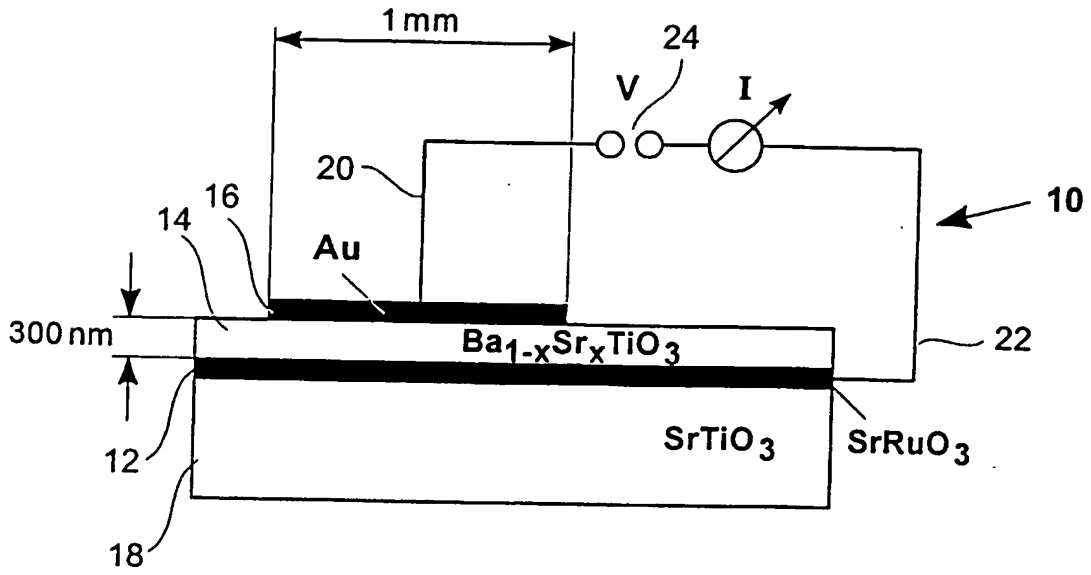

1 mm
24
V
I
20
16
14
10
Au
300 nm
$Ba_{1-x}Sr_xTiO_3$
22
12
$SrTiO_3$
$SrRuO_3$
18

Fig. 1

Fig. 2a

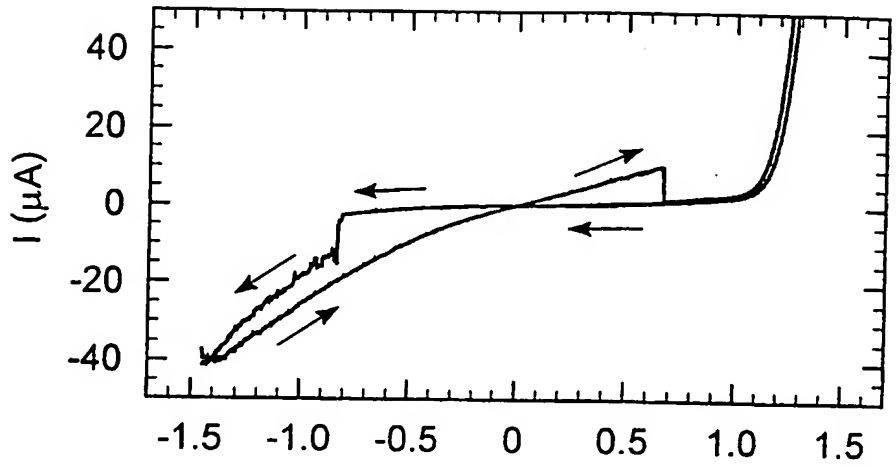


Fig. 2b

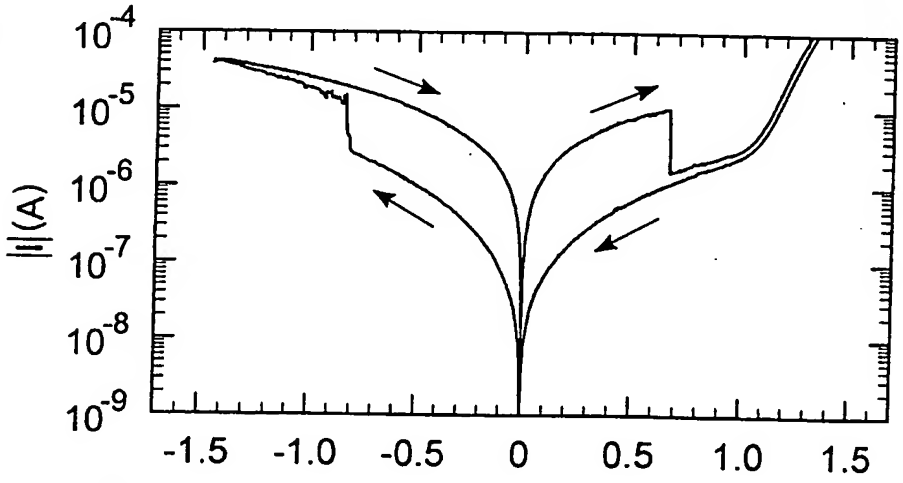
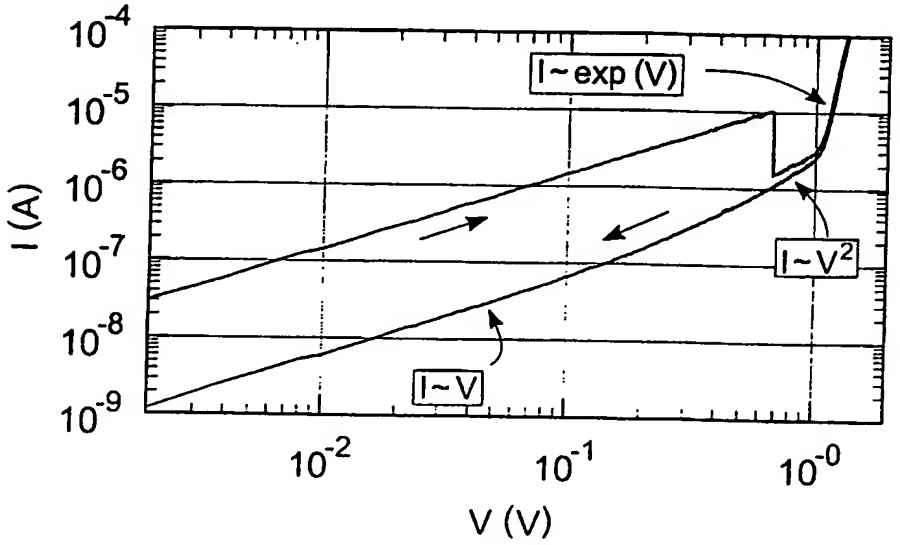


Fig. 2c



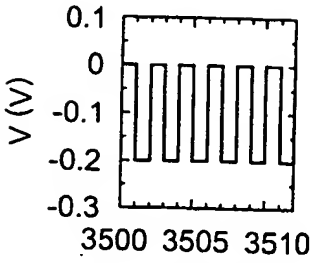


Fig. 3a

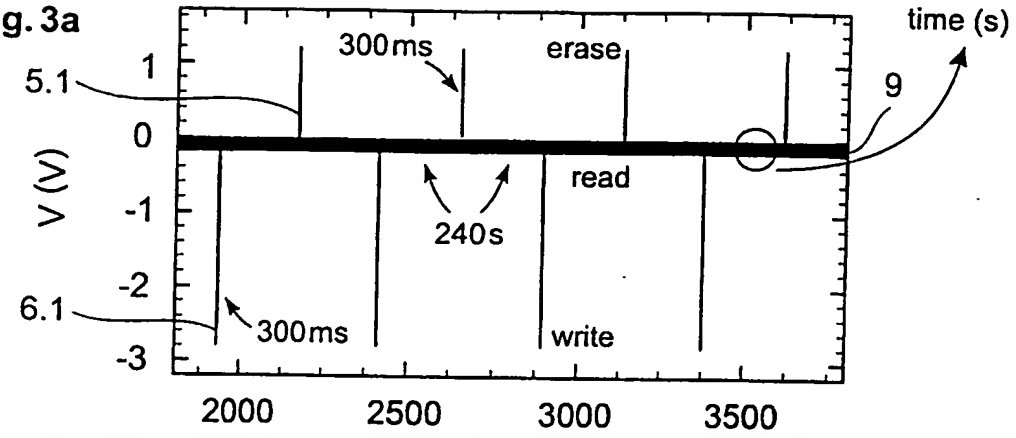


Fig. 3b

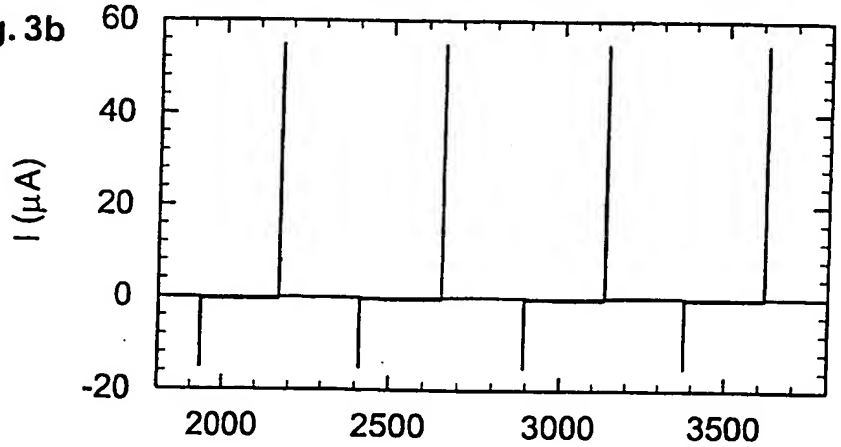


Fig. 3c

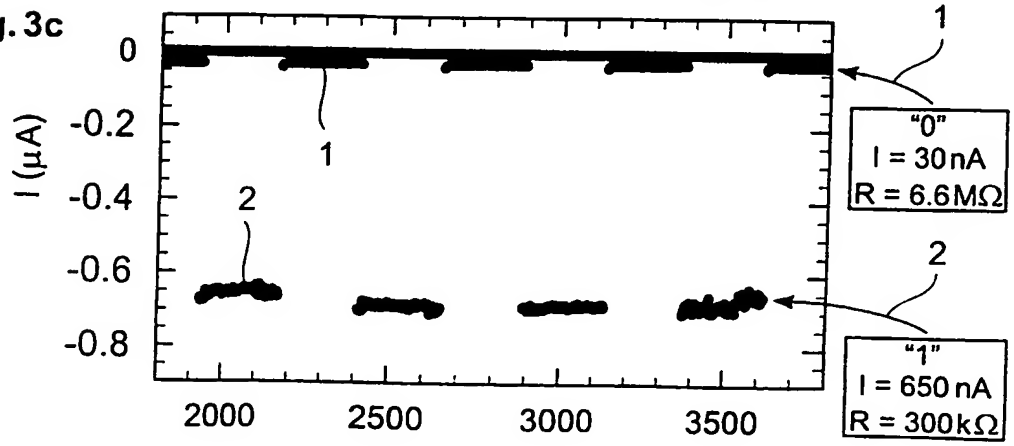


Fig. 4a

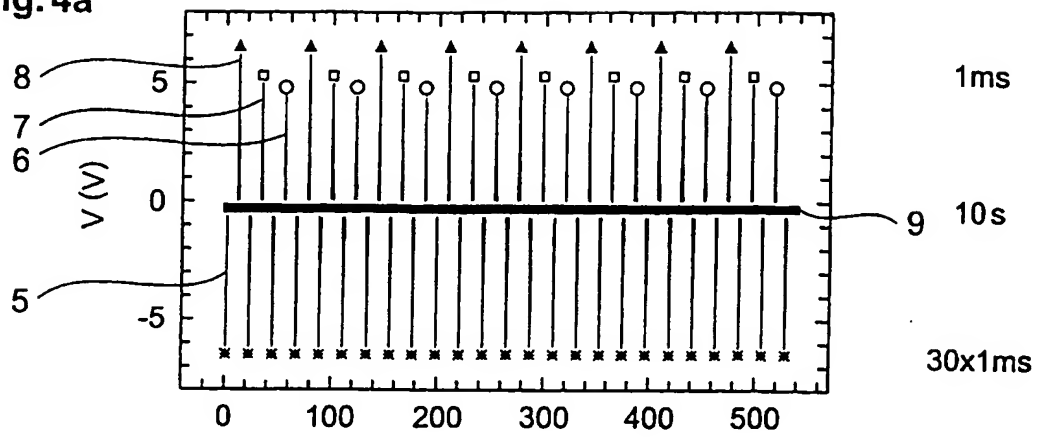


Fig. 4b

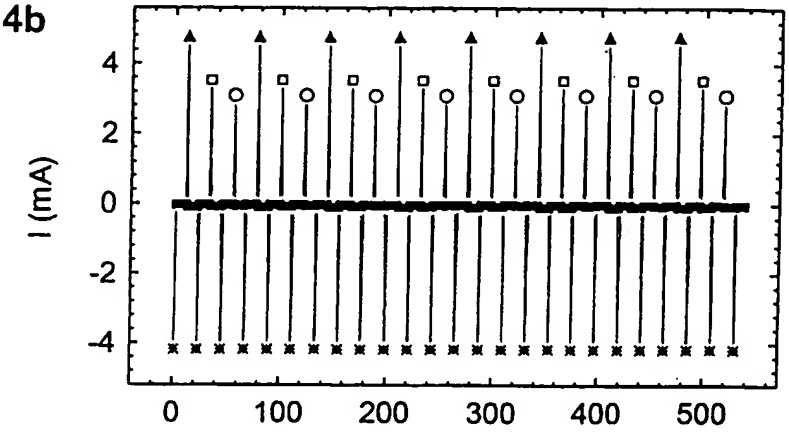
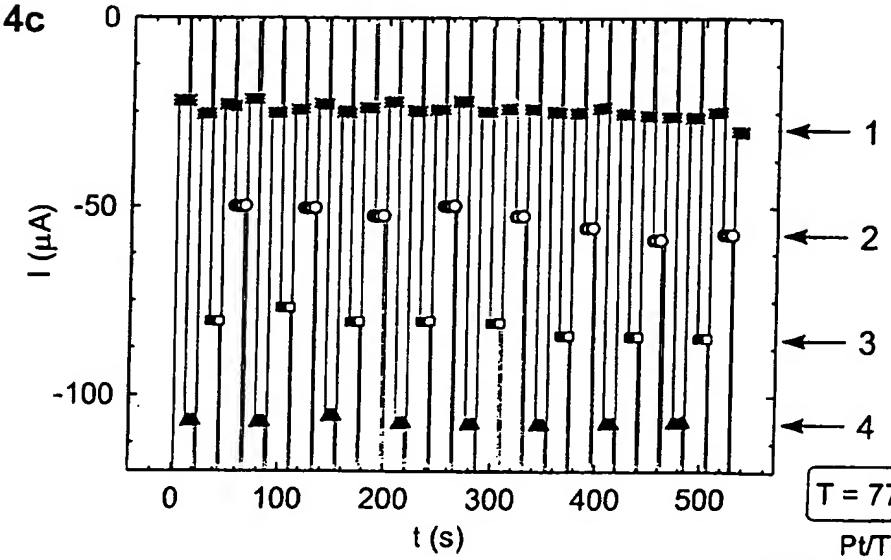
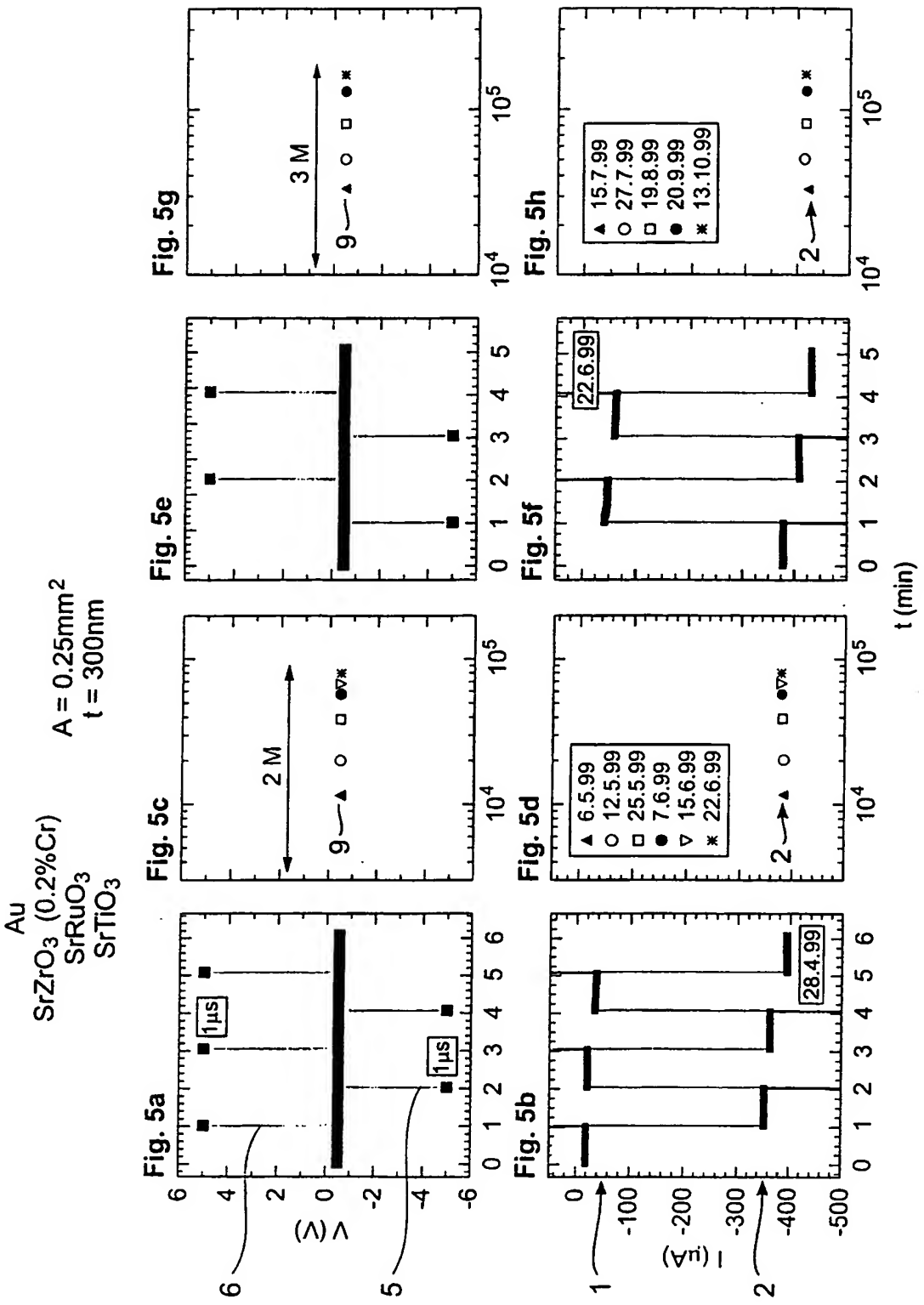


Fig. 4c



T = 77K

Pt/Ti
$SrZrO_3$ (0.2%Cr)
$SrRuO_3$
$SrTiO_3$
A = 200μm x 200 μm
t = 300nm


Au
SrZrO3 (0.2%Cr)
SrRuO3
SrTiO3
A = 0.25mm2
t = 300nm
Fig. 5a
Fig. 5b
Fig. 5c
Fig. 5d
Fig. 5e
Fig. 5f
Fig. 5g
Fig. 5h
V (V)
I (μA)
t (min)
1μs
2 M
3 M
6.5.99
12.5.99
25.5.99
7.6.99
15.6.99
22.6.99
28.4.99
15.7.99
27.7.99
19.8.99
20.9.99
13.10.99

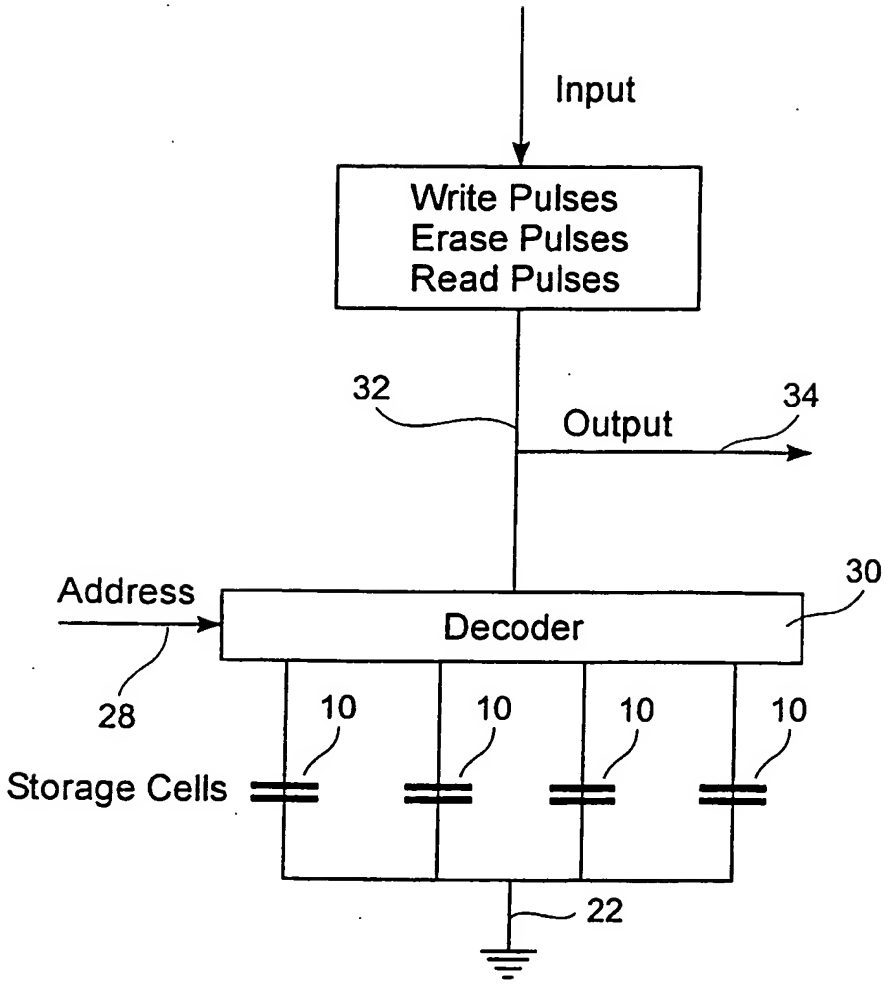

Input
Write Pulses
Erase Pulses
Read Pulses
32
Output
34
Address
30
Decoder
28
10
10
10
10
Storage Cells
22

Fig. 6

INTERNATIONAL SEARCH REPORT

Int. ..tional Application No
PCT/IB 00/00043

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/115 H01L29/51 G11C11/22 C04B35/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L C04B G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 623 439 A (YOSHIDA AKIRA ET AL) 22 April 1997 (1997-04-22) figures 1-3,5-8 column 2, line 59 -column 3, line 46 column 4, line 15 -column 6, line 31 column 6, line 65 -column 8, line 55	1,2,4, 7-9,12, 17-20, 22,24-26
Y		3,5,6, 21,23
A		10,11, 13-16

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 March 2000	29/03/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Polesello, P

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Int. ional Application No
PCT/IB 00/00043

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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A		2-6

X	US 4 767 729 A (OSMAN MAGED A ET AL) 30 August 1988 (1988-08-30) column 2, line 53 -column 5, line 19	1,8,11, 13,18, 25,26
A		2-7

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A	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 06, 30 April 1998 (1998-04-30) -& JP 10 036171 A (SONY CORP), 10 February 1998 (1998-02-10) abstract; figures 1,2	1-9, 12-15, 17-26

A	YUKIO WATANABE: "EPITAXIAL ALL-PEROVSKITE FERROELECTRIC FIELD EFFECT TRANSISTOR WITH A MEMORY RETENTION" APPLIED PHYSICS LETTERS,US,AMERICAN INSTITUTE OF PHYSICS. NEW YORK, vol. 66, no. 14, 3 April 1995 (1995-04-03), pages 1770-1772, XP000500955 ISSN: 0003-6951 figures 1-3 page 1770, column 2, line 13 -page 1771, column 2, line 32	1-4,8, 10, 17-22, 24-26

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INTERNATIONAL SEARCH REPORT

Int. ..tional Application No
PCT/IB 00/00043

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	AUCIELLO O ET AL: "The physics of ferroelectric memories" PHYSICS TODAY, JULY 1998, AIP, USA, vol. 51, no. 7, pages 22-27, XP002108793 ISSN: 0031-9228 cited in the application figures 1B,2,3 page 22, column 2, line 24 page 23, column 1, line 10 -column 2, line 16 page 25, column 1, line 2 - line 8 page 25, column 2, line 9 - line 14 box 1, page 24 ---	1-9,12, 17-26
A	US 5 840 110 A (AZUMA MASAMICHI ET AL) 24 November 1998 (1998-11-24) figures 1-8,11-18,29-37 column 3, line 1 -column 6, line 65 column 13, line 57 -column 16, line 41 examples 9,10 ---	1-9, 14-26
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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int. ..tional Application No
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